UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/536,452	03/28/2000	Ronny Ronen	02207/8754	5160

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SUITE 700	2183	
WASHINGTON, DC 20005		

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/536,452	RONEN ET AL.
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,7-9,11-15,17,18 and 22-28* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,7-9,11,13-15,17,18,22,and 25-28* is/are rejected.

7)☒ Claim(s) *12,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some *   c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-2, 4, 7-9, 11-15, 17-18, and 22-28 have been examined.

Papers Submitted

2.   It is hereby acknowledged that the following papers have been received and placed of

record in the file: Amendment and Extension of Time as received on 8/29/2005.

Claim Objections

3.   Claim 27 is objected to under 37 CFR 1.75(c), as being of improper dependent form for

failing to further limit the subject matter of a previous claim. Applicant is required to cancel the

claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the

claim(s) in independent form. Claim 27 is dependent on claim 12. Claim 12 essentially states

that a flag is generated only if A and B (note that A and B are symbolic of the actual claim

limitations). Or, as long as A and B are true, then no matter what else happens, the flag is

generated. Claim 27 then states that a flag is generated if A, B, and C. Or, as long as A and B

are true, if C is also true, the flag is generated. This is inherently covered by claim 12 since

claim 12 is only concerned with A and B (C may or may not exist and the system of claim 12

does not care).

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

5.   Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention. Since claim 27 includes the limitations of claim 12 (due to dependency), claim 27

is not clear because its scope is unclear. More specifically, claim 12 states that a flag is

generated only if A and B are true (A and B being symbolic of the actual limitations). Claim 27

then states that the flag is generated if A, B, and C are true. Does applicant want to generate a

flag if A, B, and C are true and not only if A and B are true? If so, then this is not clear because

the limitation of claim 12 must still hold. If not, then it is not clear why applicant introduces

element C, when all that matters are elements A and B. Does applicant really intend for claim 27

to be dependent on claim 12, or should it be dependent on another claim?

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7.   Claims 1-2, 4, 7-9, 11, 13-15, 17-18, 22, 25-26, and 28 are rejected under 35

U.S.C. 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 (as applied in the

previous Office Action and herein referred to as Killian).

8.   Referring to claim 1, Killian has taught a processor comprising:

a) means for executing an instruction of an application of a first bit size ported to a second bit

size environment, the second bit size being greater than the first bit size. See column 2, lines 7-

33.

b) means for confining the application to an address space subset of the first bit size (see column

19, lines 36-40), said means for confining comprising:

  (i) means for truncating generated address references of the second bit size to the first bit

  size. See Fig.5D and note that the 64-bit virtual address is truncated by removing the

  upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.

  (ii) means for determining that the address space subset of the first bit size is signed

  address space or unsigned address space based on a setting of an address format control

  signal, the address format control signal having a first setting to indicate unsigned address

  space and a second setting to indicate signed address space. When in 32-bit mode, bits in

  the status register signal to the system whether the 32-bit mode is 32-bit user mode or 32-

  bit kernel/supervisor mode. See column 17, lines 25-27. With one signal setting (32-bit

  user mode), the system deals only with unsigned address space (positive addresses). See

  column 17, line 66, to column 18, line 1. Also, see Fig.3A and note the unsigned address

  space in 32-bit user mode. With a second signal setting (32-bit kernel/supervisor mode),

  the system deals with signed address space. See column 19, lines 30-33, and column 3,

  lines 38-55. That is in kernel/supervisor mode, both user and kernel/supervisor address

  may be accessed (negative and positive addresses).

  (iii) means for extending to the second bit size the truncated generated address references

  based on results from said means for determining, zero-extending the truncated generated

address references if the address space of the first bit size is unsigned and sign-extending

the truncated generated address references if the address space subset of the first bit size

is signed. See column 17, lines 61-68, and note that in 32-bit user mode (unsigned

space), the upper 32-bits are always forced to zero (zero-extension). Furthermore, see

column 18, lines 8-17, and note that when in 32-bit kernel/supervisor mode (signed

space), addresses are sign-extended. Since, the mode is determined by the status register

signal, the type of extension is also determined by the signal.

9.   Referring to claim 2, Killian has taught a processor as described in claim 1. Killian has

further taught that the first bit size is 32-bit and the second bit size is 64-bit. See column 3, lines

30-31, and column 5, lines 8-19.

10.   Referring to claim 4, Killian has taught a processor as described in claim 1. Killian has

further taught that the means for confining includes means for generating an address fault. See

column 11, lines 3-5. The 32-bit address (which would be represented as an extended 64-bit

number in the 64-bit environment) that is used to select a memory location in the address space

subset is checked for a certain value and if that value exists, then an address error exception will

occur.

11.   Referring to claim 7, Killian has taught a processor comprising:

a) a memory to store an instruction of an application ported from a first bit size environment to a

second bit size environment, the second bit size being greater than the first bit size. See Fig.1

and column 7, lines 49-54. Note the existence of main memory and an instruction cache.

b) an instruction execution core coupled to said memory, said instruction execution core to

execute the instruction of the application. See Fig.1. Note that data and instructions are

retrieved from memory/cache by the EIC (component 25) and propagated along bus 30 to the

execution unit.

c) said instruction execution core to determine that the application is confined to an address

space subset of the first bit size. See column 19, lines 36-40.

d) said instruction execution core to generate an address reference of the second bit size as part

of execution of the instruction. See column 12, lines 26-65. Also, see Fig.5D and note that a

virtual address is generated (at the middle of the page).

e) said instruction execution core to truncate the generated address reference from the second bit

size to the first bit size. See Fig.5D and note that the 64-bit virtual address is truncated by

removing the upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.

f) said instruction execution core to determine that the address space subset of the first bit size is

signed address space or unsigned address space based on a setting of an address format control

flag, the address format control flag having a first setting to indicate unsigned address space and

a second setting to indicate signed address space. When in 32-bit mode, bits in the status register

signal to the system whether the 32-bit mode is 32-bit user mode or 32-bit kernel/supervisor

mode. See column 17, lines 25-27. With one signal setting (32-bit user mode), the system deals

only with unsigned address space (positive addresses). See column 17, line 66, to column 18,

line 1. Also, see Fig.3A and note the unsigned address space in 32-bit user mode. With a second

signal setting (32-bit kernel/supervisor mode), the system deals with signed address space. See

column 19, lines 30-33, and column 3, lines 38-55. That is in kernel/supervisor mode, both user

and kernel/supervisor address may be accessed (negative and positive addresses).

g) said instruction execution core to zero-extend the truncated, generated address reference to the second bit size if the address space of the first bit size is determined to be unsigned address space. See column 17, lines 61-68, and note that in 32-bit user mode (unsigned space), the upper 32-bits are always forced to zero (zero-extension).

h) said instruction execution core to sign extend the truncated, generated address reference to the second bit size if the address space subset of the first bit size is determined to be signed address space. See column 18, lines 8-17, and note that when in 32-bit kernel/supervisor mode (signed space), addresses are sign-extended. Since, the mode is determined by the status register signal, the type of extension is also determined by the signal.

12.   Referring to claim 8, Killian has taught a processor as described in claim 7. Killian has further taught that the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment. See column 3, lines 30-31, and column 5, lines 8-19.

13.   Referring to claim 9, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to determine that the application is confined to the address space subset of the first bit size based at least in part on an address space control flag. See column 17, lines 25-27. Note from columns 17-19, that based on the different modes, different address space subsets are used.

14.   Referring to claim 11, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference. Recall from previous rejections that a generated 32-bit number is extended to

a 64-bit number in Killian's system. From column 17, line 61, to column 18, line 7, Killian has

disclosed that bit 31 of the 64-bit number is checked. If that value is 0, then an address fault has

not occurred. However, if that value is 1, then an address exception has occurred. Bit 31, in a

sense, represents an overflow bit in that when that bit is set, then the 32-bit application has

crossed the 32-bit address space boundary and a fault has occurred. It should be noted that a

comparison would inherently be performed to check bit 31. And, this comparison is related to

both the original 32-bit address and the extended 64-bit version.

15.   Referring to claim 13, Killian has taught a processor as described in claim 7. Killian has

further taught that the memory is a cache memory. See column 7, lines 50-52.

16.   Referring to claim 14, Killian has taught a processor as described in claim 7. Killian has

further taught that the processor is a 64-bit processor. See column 2, lines 16-41, and column 3,

lines 30-31. Killian has disclosed that the registers and data path, along with memory addresses,

are 64 bits wide. Therefore, Killian has taught a 64-bit processor.

17.   Referring to claim 15, the method of claim 15 is performed by the processor of claim 7.

Therefore, claim 15 is rejected for the same reasons set forth in the rejection of claim 7.

18.   Referring to claim 17, Killian has taught a method as described in claim 15.

Furthermore, the method of claim 17 is performed by the processor of claim 8. Consequently,

claim 17 is rejected for the same reasons set forth in the rejection of claim 8.

19.   Referring to claim 18, Killian has taught a method as described in claim 15.

Furthermore, the method of claim 18 is performed by the processor of claim 9. Consequently,

claim 18 is rejected for the same reasons set forth in the rejection of claim 9.

20.   Referring to claim 22, Killian has taught a method as described in claim 15.

Furthermore, the method of claim 22 is performed by the processor of claim 11. Consequently,

claim 22 is rejected for the same reasons set forth in the rejection of claim 11.

21.   Referring to claim 25, Killian has taught a processor as described in claim 2. Killian has

further taught that the unsigned address space is 4 gigabytes and the signed address space is -2

gigabytes to +2 gigabytes. As described above, when in 32-bit mode, bits in the status register

signal to the system whether the 32-bit mode is 32-bit user mode or 32-bit kernel/supervisor

mode. See column 17, lines 25-27. With one signal setting (32-bit user mode), the system deals

only with unsigned address space (positive addresses). See column 17, line 66, to column 18,

line 1. Also, see Fig.3A, which shows the unsigned address space in 32-bit user mode (note that

4GB of space exists even though only 2GB of the 4GB are accessible). With a second signal

setting (32-bit kernel/supervisor mode), the system deals with signed address space. See column

19, lines 30-33, and column 3, lines 38-55. That is in kernel/supervisor mode, both user and

kernel/supervisor address may be accessed (negative and positive addresses from -2GB to

+2GB).

22.   Referring to claim 26, Killian has taught a processor as described in claim 8.

Furthermore, claim 26 is rejected for the same reasons set forth in the rejection of claim 25.

23.   Referring to claim 28, Killian has taught a method as described in claim 17.

Furthermore, the method of claim 28 is performed by the processor of claim 25. Consequently,

claim 28 is rejected for the same reasons set forth in the rejection of claim 25.

Allowable Subject Matter

24.   Claims 12, 23, and 24 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims.

Response to Arguments

25.   Applicant's arguments filed on August 29, 2005, have been fully considered but they are

not persuasive.

26.   Applicant argues the novelty/rejection of claim 1 on page 7 of the remarks, in substance

that:

> "...However, while this may constitute zero-extension of VA(31..0), there is no sign extension of
> this truncated address. It is assumed that any 32-bit address presented to the address
> translation mechanism is in sign extended form (see Killian col. 18, lines 11-17), such that there is
> no sign extension of the truncated address bits in 32-bit kernel mode."

27.   These arguments are not found persuasive for the following reasons:

a) According to Fig.5D and column 18, lines 13-15, of Killian, all 32-bit addresses are presented

to the address translation circuit, regardless of the mode. If the address is already assumed to be

sign extended, then when the sign bit is 0, the upper 32 zero-bits of the virtual address are

truncated and passed to the right input of multiplexer 172. Similarly, if the sign bit is 1, the

upper 32 one-bits of the virtual address are truncated and passed to the right input of multiplexer

172. In either case, sign bits are truncated and sent to the right input of the multiplexer. In

addition, as shown in the Figure, 32-zeroes are passed to the left input of multiplexer 172 in case

32-bit user mode is selected. Therefore, the following options will occur:

a) In 32-bit user mode, the left input of multiplexer 172 is selected and 32 zeros are

appended to the address, thereby zero-extending the address.

b) If the upper 32 bits of the virtual address are zeros, then those zeros are sent to the

right input of multiplexer 172, thereby truncating the address. If the system is not in 32-

bit user mode, the right input of multiplexer 172 would be selected and the 32 zeros that

were truncated are now appended to the address, thereby sign-extending the address

(since the appended bits are the sign bits).

c) If the upper 32 bits of the virtual address are ones, then those ones are sent to the right

input of multiplexer 172, thereby truncating the address. If the system is not in 32-bit

user mode, the right input of multiplexer 172 would be selected and the 32 ones that were

truncated are now appended to the address, thereby sign-extending the address (since the

appended bits are the sign bits).

Consequently, Killian has taught sign-extending truncated addresses.

28.   Applicant argues the novelty/rejection of claim 1 on pages 7-8 of the remarks, in

substance that:

> "Applicants understand the Examiner's position to be that the user virtual address space, as
> illustrated in Fig.3A of Killian, constitutes an unsigned address space since VA(31)=0 for the 32-
> bit user mode addresses. Even so, this is not an address space of the first bit size, but an
> address space of the first bit size minus one. For example, whereas in Killian a 32-bit instruction
> in 32-bit user mode can address 0-2 GB and in 32-bit kernel mode can address -2GB to +2GB, in
> a 32-bit application ported to a 64-bit environment embodiment of the present invention, the 32-bit
> application can operate within an unsigned 0 to 4GB, and within signed -2GB to +2 GB."

29.   These arguments are not found persuasive for the following reasons:

a) The examiner asserts that applicant is reading the claim too narrowly. The claim requires that

an application be confined to an address space subset of the first bit size. Killian does in fact

teach this. Looking at Fig.3A, and column 10, lines 51-61, addresses can be generated with

bit(31) = 0 or 1, thereby confining the application to a full 32-bit address space subset. Now, it is

true that bit(31)=1 will generate an error, but the addresses may be generated, and this allows for

generation of 2^{32} addresses which correspond to a 2^{32} size address space and no more. On the

other hand, it should also be realized that being confined to a first subset within a second subset

still results in being confined to the second subset. In other words, if a person were to be

confined to his house, and more specifically, confined to the kitchen of his house, then that

person is not only confined to the kitchen but also confined to (kept within) the house. Similarly,

in Killian's 32-bit user mode, an application is confined to the address space (0 to 2^{32} - 1) shown

in Fig.3A, and more specifically, is confined to a subset (0 to 2^{31} - 1) of the address space (0 to

2^{32} - 1) shown in Fig.3A. But, as demonstrated in the hypothetical above, the application is still

confined to the superset (or 2^{32} - 1 address spaces).

30.   Applicant argues the novelty/rejection of claim 11 on page 8 of the remarks, in substance

that:

> "...generation of an address exception in Killian is an absolute based on whether bit VA(31) is
> one, which equals overflow. There is no comparison of the generated reference with the
> extended, truncated generated address reference."

31.   These arguments are not found persuasive for the following reasons:

a) From Fig.5D, it can be seen that the address is sent to logic 170, which as shown in Fig.5E,

checks for overflow errors. The examiner asserts that a comparison, at some level, must exist.

The logic of the system will operate as follows:

if ((32-bit user mode = = 1) && (VA(31) = = 1))
        generate R0ERR (overflow error) ;

So, there is a comparison of some sorts. The signal must be checked to see whether it is a 1 or a

0 (compared to a 1 of 0) and based on the outcome, either generate an error or not.

Conclusion

32.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168.

The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
October 20, 2005

RICHARD L. ELLIS
PRIMARY EXAMINER